60W L-BAND POWER AlGaAs/GaAs HETEROSTRUCTURE FETs

Junko Morikawa, Kazunori Asano, Kohji Ishikura,
Hirokazu Oikawa, *Mikio Kanamori and Masaaki Kuzuhara

ULSI Device Development Laboratories, NEC Corporation
*Kansai Electronics Research Laboratories, NEC Corporation
9-1, Seiran 2-Chome, Otsu, Shiga 520, Japan

Abstract

This paper describes DC and RF power performance of a newly-developed high-power AlGaAs/GaAs heterostructure FET (HFET)[1] designed for L-band SSPA applications. A push-pull power amplifier, composed of two HFET chips, demonstrated state-of-the-art power performance of 60W output-power with a power-added effkiency (PAE) of 54 % at 1 .5GHz.

Introduction

With the recent world-wide progress in personal communication systems, there is an increasing requirement for developing small-sized SSPAs for use in digital cellular base stations. For such applications, the development of high-power RF devices with high-efficiency is of primary significance.

Since HFETs have higher Schottky barrier height than GaAs MESFETs, the HFET enables us to achieve improved gate breakdown voltage (BV_{gd}) with reduced gate leakage current, which is of principal importance for high-power applications. Furthermore, the HFET structure is inherently suited for precise recess-depth control, reflecting the structural advantage of selective dry-etching capability between AlGaAs and GaAs.

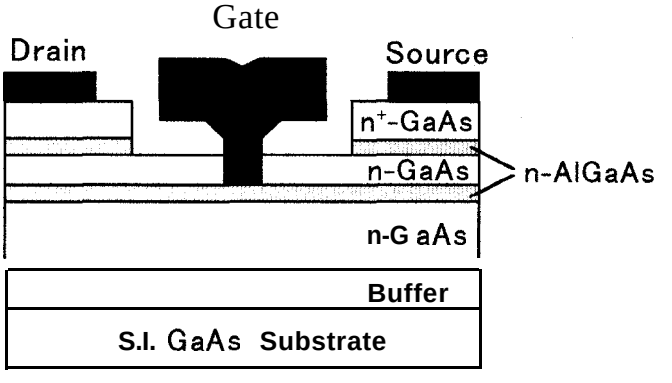

Figure 1. Schematic cross sectional view of developed HFETs.

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In this paper, L-band power performance of a newly-developed 60W AlGaAs/GaAs HFET amplifier is described.

Design and Fabrication Process of HFET

A schematic cross section of the fabricated HFET is shown in Figure 1. The active part of the HFET structure consists of a Si-doped n-type AlGaAs Schottky layer and a Si-doped n-type GaAs channel layer. The doping concentration of the AlGaAs Schottky layer and the channel layer was chosen to be $2.0 \times 10^{17} cm^{-3}$. The thickness and concentration are designed to achieve optimal $I_{,,}$ and BV_{gd}. To control the depth of the wide recess,

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a 5nm-thick Si-doped AlGaAs stopper layer was introduced just beneath the n^+-GaAs contact layer. The device structure includes a 3 .O μm wide recess, selectively-etched into the n^+-GaAs contact layer using a BCl_3/SF_6 mixture gas. Since the wide recess surface in our structure is covered with GaAs, instead of AlGaAs, undesirable surface phenomena under large-signal operation related to AlGaAs deep-levels can be suppressed, leading to improved power performance in the saturation region. The device structure also includes a 1.0 μm narrow recess selectively-etched into the n-GaAs layer on the AlGaAs Schottky layer as a dry-etching stopper for the narrow recess. A Buried WSi Schottky gate with a gate length of 1.0 μm was formed in the narrow recess region. Alloyed AuGe/Ni contacts were employed for source and drain ohmic electrodes. To ensure low thermal resistance, the GaAs substrate was properly thinned and a plated-heat-sink (PHS) was formed on the back side of it.

HFET Performance

Typical I-V characteristics for a unit HFET (l-finger HFET, Wg=100 μm) are illustrated in Figure 2, which shows excellent DC saturation and pinch-off characteristics with a maximum drain current of 400mA/mm. Figure 3 shows the transconductance (gm) measured as a function of gate voltage for a unit HFET at Vds=2.0V. A constant gm of 1 10mS/mm is observed. The gate breakdown voltage was higher than 23V. Figure 4 shows a plot of uniformity in the threshold voltage (V_{th}) estimated on an entire 3-inch wafer. The standard deviation of V_{th} was 40mV, which is less than 1/3 of that obtained for the conventional MESFET.

Figure 5 shows I,, as a function of BV_{gd} of a single-chip HFET with a gate-width (Wg) of 43mm. The HFET exhibited more than 2A higher I,, than MESFET with an identical BV_{gd}.

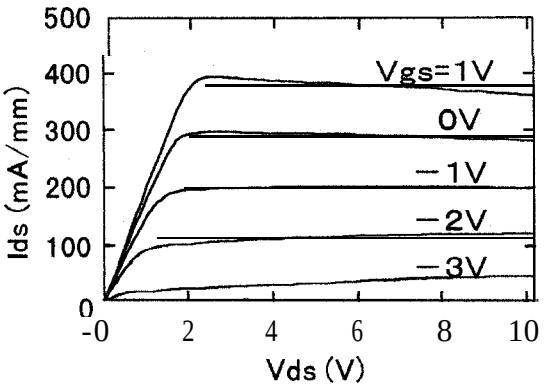

Figure 2. Id-Vd charactaristics of HFET.

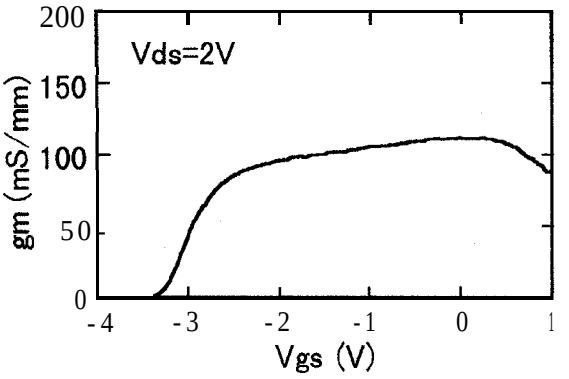

Figure 3. Transcondactance as a function of gate voltage.

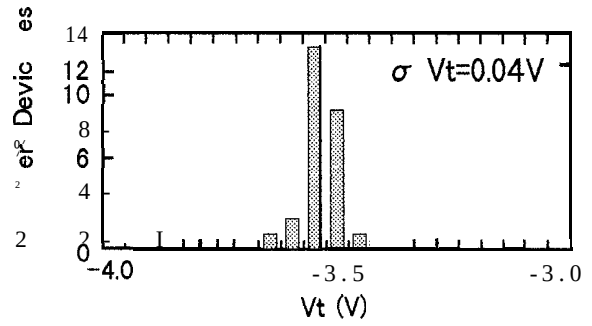

Figure 4. Vt distribution of HFET

Measured output power (P_{out}) and PAE as a function of input power (P_{in}) at 1.5GHz are shown in Figure 6. Data were taken using an external tuning technique. The device achieved an output-

power of 25.5W with PAE of 50 % at a drain bias voltage (V_{DS}) of 10V. The output-power level was higher by more than 5W than that for a conventional GaAs MESFET with identical electrode configuration.

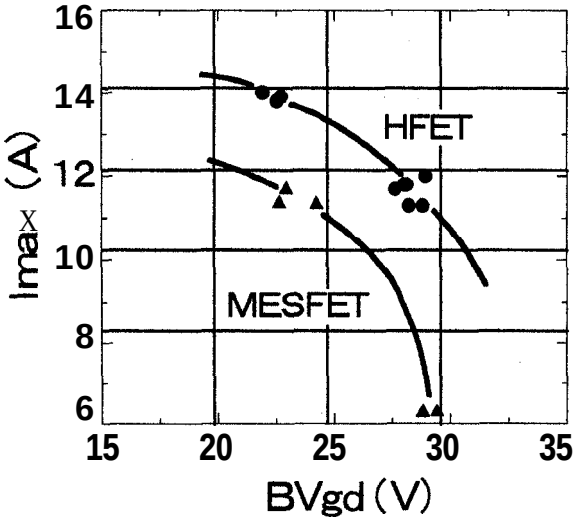

Figure 5. Imax versus BVgd of HFET(Wg=43mm).

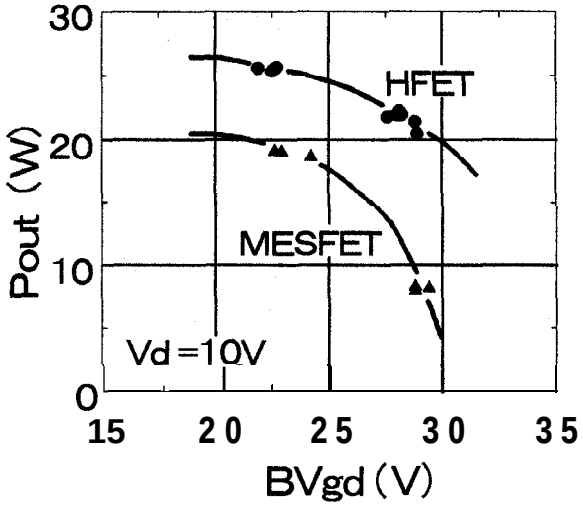

Figure 6. Output power versus BVgd at 1.5GHz (Wg=43mm).

To obtain much higher Pout, two chip parallel operation was examined. With an increase in total Wg, however, power combining loss generally increases because of the increase in phase mismatch and impedance transforming loss. In order to solve this trade-off problem, a push-pull configuration was employed[2]. Figure 7 shows the overall push-pull circuit. The amplifier was matched to 50 ohm at the input and output ports with 2:1 balun transformers, impedance matching capacitors and transmission lines. The fabricated push-pull amplifier is composed of two HFET chips (Wg=2 x 66 mm). Figure 8 is a photograph of Wg=66mm HFET chip. The amplifier, power-tested at 1.5GHz, achieved P_{out} of 47.8dBm (60W) at a 2dB gain compression point with a PAE of 54 % and a linear gain of 13.7dB at V_{DS}=10V as shown in Figure 9. At V_{DS}=11V, the amplifier exhibited 48.2dBm (66W). To our knowledge, these results are the best output-power performance achieved to date employing AlGaAs/GaAs HFET technology.

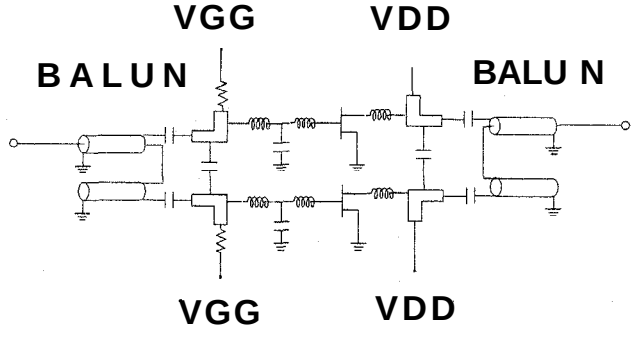

Figure 7. Push-pull amplifier circuit

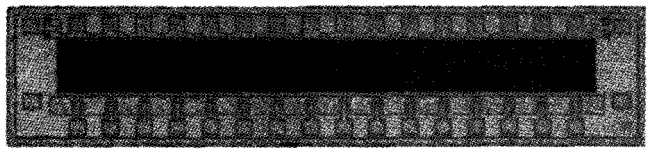

Figure 8. Photograph of Wg=66mm HFET chip.

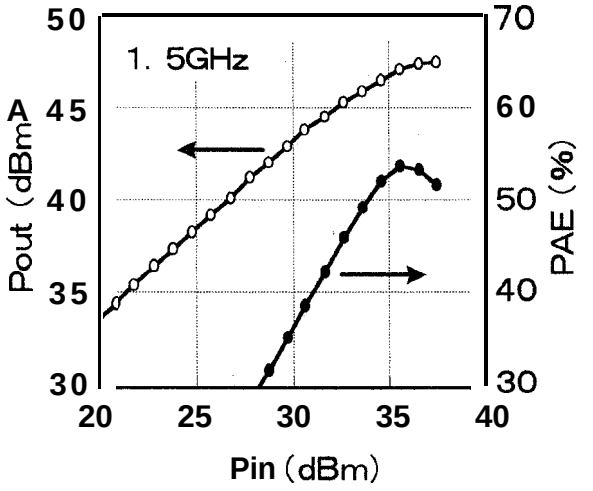

Figure 9. Output Power and drain efficiency as a function of input power (Wg = 2 x 66 mm).

Conclusions

L-band high power GaAs HFETs have been developed. At 1 .5GHz, an output power of 60W has been obtained with 54 % power-added efficiency. The developed HFET is promising for use in digital cellular base station systems.

Acknowledgments

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References

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